WHAT IS CLAIMED IS:

1. A method for reducing transfer latencies in fencepost buffering comprising the steps of:

providing a cache between a network controller and a host entity with shared memory wherein the cache has a top cache and a bottom cache;

fetching a first and second descriptor address location from shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor;

copying the active descriptor to the top cache; and

issuing a command to DMA for transfer of the active descriptor.

2. The method of Claim 1 further comprising the step of copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.

3. The method of Claim 2 further comprising the steps of:

fetching a next descriptor address location from external memory; and

placing the next descriptor address location in the second descriptor address location.

4. The method of Claim 1 further comprising the step of updating the ownership of terminal descriptors.

5. The method of Claim 4 wherein the step of updating the ownership of the terminal descriptors further comprises the step of writing an End of Frame (EOF) descriptor to shared memory before writing a Start of Packet (SOP) descriptor to shared memory.

6. The method of Claim 5 further comprising the step of setting an ownership bit in the EOF descriptor when the EOF descriptor is the active descriptor.

7. The method of Claim 6 further comprising the steps of:

reediting the active descriptor to build an image of the SOP descriptor;

copying the SOP descriptor to the bottom cache; and

issuing a command to the DMA requesting transfer of the SOP descriptor to shared memory.

8. A method for reducing transfer latencies in fencepost buffering having chained descriptors comprising the steps of:

providing a cache between a host and a network controller having local memory wherein the cache has a top cache and a bottom cache;

fetching a first and second descriptor address location from shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor; and

updating the ownership of terminal descriptors by writing an End of Frame (EOF) descriptor to shared memory before writing a Start of Package (SOP) descriptor to shared memory;

issuing a command to DMA for transfer of the active descriptor.

9. The method of Claim 8 wherein the step of updating the terminal descriptors further comprises the steps of:

reediting the active descriptor to build an image of the SOP descriptor; and

copying the SOP descriptor to the bottom cache.

10. The method of Claim 9 further comprising the step of transferring the bottom cache to shared memory.

11. The method of Claim 8 further comprising the step of copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.

12. The method of Claim 11 further comprising the steps of:

fetching a next descriptor address location from external memory; and

placing the next descriptor address location in the second descriptor address location.

13. A system for reducing transfer latencies in fencepost buffering having chained descriptors comprising:

a network controller;

a host entity with shared memory;

a cache between said network controller and said host entity with shared memory wherein the cache has a top cache and a bottom cache;

means for fetching a first and second descriptor address location from shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor;

means for updating the ownership of terminal descriptors by writing an End of Frame (EOF) descriptor to shared memory before writing a Start of Package (SOP) descriptor to shared memory; and

means for issuing a command to DMA for transfer of the active descriptor.

14. The system of Claim 13 wherein the means for updating the terminal descriptors further comprises:

means for reediting the active descriptor to build an image of the SOP descriptor; and

means for copying the SOP descriptor to the bottom cache.

15. The system of Claim 14 further comprising means for transferring the bottom cache to shared memory.

16. The system of Claim 13 further comprising means for copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.

17. The system of Claim 16 further comprising:

means for fetching a next descriptor address location from external memory; and

means for placing the next descriptor address location in the second descriptor address location.